What is claimed is :

1. A semiconductor packaging structure comprising:

an electrically substrate having a top surface and a bottom surface;

a semiconductor die uplying said top surface;

a first array comprising a first plurality of solder joints and a second plurality of solder joints, mounted on said die surface and projecting downwardly, therefrom, said first plurality of solder joints having a higher melting point than said second plurality of solder joints; and

a second array comprising a third plurality of solder joints; mounted on said top surface, integral with said first array, therefrom, connecting said die surface and said top surface, and said third plurality of solder joints having a higher melting point than said second plurality of solder joints.

2. The structure described in claim 1 further comprising:

a group of solder paste located between said first array and said and said second array; said first array integral with said second array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and said third plurality of solder joints were not melted, and said second plurality of solder joints were melted.

3. The structure described in claim 1 further comprising:

a print circuit board underlying said substrate;

a third ball grid array comprising a fourth plurality of solder joints and a fifth

plurality of solder joint, mounted on said bottom surface and projecting downwardly, therefrom, said fourth plurality of solder joints having a higher melting point than said fifth plurality of solder joints; and

a fourth array comprising a sixth plurality of solder joints, mounted on said print circuit board, integral with said third array, therefrom, connecting said bottom surface and said print circuit board, and said sixth plurality of solder joints having a higher melting point than said fifth plurality of solder joints.

4. The structure described in claim 1 further comprising:

a group of solder paste located between said third array and said fourth array; said third array integral with said fourth array, at integral process, predetermined the shape of solder joints, said fourth plurality of solder joints and said sixth plurality of solder joints were not melted, and said fifth plurality of solder joints were melted.

5. The structure described in claim 1 wherein said solder joint comprising a flat surface at its front edge.

6. The structure described in claim 5 wherein said flat surface implemented on said die surface is 3% to 70% smaller than said corresponding flat surface implemented on said top surface.

7. The structure described in claim 5 wherein said flat surface implemented on said bottom surface is 3% to 70% smaller than said corresponding flat surface implemented on said print circuit board.

8. The structure described in claim 2 wherein said semiconductor package had been assembled, said first plurality of solder joints and said third plurality of solder joints were not melted; and said second plurality of solder joints and said solder paste were melted.

9. The structure described in claim 3 wherein said semiconductor package had been assembled, said fourth plurality of solder joints and said sixth plurality of solder joints were not melted; and said fifth plurality of solder joints and said solder paste were melted.

10. The structure described in claim 1 wherein said first plurality of solder joints are located at four corners of said die surface.

11. The structure described in claim 1 wherein said first plurality of solder joints are located at middle ground plane of said die surface.

12. The structure described in claim 3 wherein said fourth plurality of solder joints are located at four corners of said bottom surface.

13. The structure described in claim 3 wherein said fourth plurality of solder joints are located at middle ground plane of said bottom surface.

14. The structure described in claim 3 wherein said second plurality of solder joint having a higher or equal melting point than said fifth plurality of solder joints.

15. The structure described in claim 1 wherein the number of semiconductor dies is more than one.

16. The structure described in claim 1 wherein said solder joints implemented on said die surface are heading in correspondence with said solder joints implemented on said top surface.

17. The structure described in claim 1 wherein said solder joints implemented on said bottom surface are heading in correspondence with said solder joints implemented on said print circuit board.

18. A semiconductor packaging structure comprising:

at lease one semiconductor die;

a print circuit board underlying said dies;

a first array comprising a first plurality of solder joints and a second plurality of solder joints, mounted on said die surface and projecting downwardly; and

a fourth array comprising a sixth plurality of solder joints, mounted on said print circuit board, integral with said first array, therefrom, connecting said

die surface and said print circuit board, and said sixth plurality of solder joints having a higher melting point than said second plurality of solder joints.

19. The structure described in claim 18 further comprising:

a solder paste located between said first array and said fourth array; said first array integral with said fourth array, at integral process, predetermined the shape of solder joints, said first plurality of solder joints and said sixth plurality of solder joints were not melted, and said second plurality of solder joints were melted.